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October 11, 2000

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Re: Takashi ABE
CIRCUIT BOARD
Our Ref. Q60938

Dear Sir:

Attached hereto is the application identified above including 13 sheets of the specification, claims, 3 sheets of formal drawings, executed Assignment and PTO 1595 form, and executed Declaration and Power of Attorney.

The Government filing fee is calculated as follows:

Total claims	18	-	20	=		x	$18.00	= $.00
Independent claims	2	-	3	=		x	$80.00	= $.00
Base Fee								$710.00
TOTAL FILING FEE								**$710.00**
Recordation of Assignment								$40.00
TOTAL FEE								**$750.00**

Checks for the statutory filing fee of $710.00 and Assignment recordation fee of $40.00 are attached. You are also directed and authorized to charge or credit any difference or overpayment to Deposit Account No. 19-4880. The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 and 1.17 and any petitions for extension of time under 37 C.F.R. § 1.136 which may be required during the entire pendency of the application to Deposit Account No. 19-4880. A duplicate copy of this transmittal letter is attached.

Priority is claimed from December 2, 1999 based on Japanese Application No. 11-343955. The priority document is enclosed herewith.

Respectfully submitted,
SUGHRUE, MION, ZINN,
MACPEAK & SEAS, PLLC
Attorneys for Applicant

By: _____
J. Frank Osha
Registration No. 24,625

CIRCUIT BOARD

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a circuit board, particularly relates to a circuit board wherein electronic parts and electrical components are mounted on the surface of a substrate such as a semiconductor chip.

Description of the Related Art

Currently, a circuit board is used for various electric equipment and information equipment. In a conventional circuit board, electronic parts are mounted on the top surface or the bottom surface of a substrate. As recent electric equipment and information equipment are miniaturized and are provided with high functions, technique for further integrating mounted electronic parts, forming a pattern of a few layers inside a circuit board and forming a circuit wherein these patterns are mutually connected has been also enhanced.

Such technique has been remarkably developed for a circuit board particularly used for a computer, however, as a digital signal is conducted in a circuit board used for this technical field, an electromagnetic wave is emitted from the circuit board as EMI noise. As EMI noise has an effect upon another circuit provided to the same electric equipment and information equipment or another electric equipment and information equipment, it is required to be reduced.

To prevent EMI noise from leaking outside the chassis of

electric equipment and information equipment, a conductive sheet was arranged inside the chassis of electric equipment and the information equipment or the chassis was made of conductive material as a major conventional technique. Also, for another technique to reduce EMI noise in the electric equipment and the information equipment on which many circuit boards are mounted, a shield plate for shielding an electromagnetic wave was provided between circuit boards, or the surface of a circuit board is shielded in a state that electronic parts are mounted.

However, it has been difficult to reduce EMI emitted noise as the performance of electric equipment and information equipment is enhanced. Emitted EMI noise cannot be reduced by only applying the shield to the chassis of electric equipment and information equipment. Therefore, a method of directly reducing emitted EMI noise caused from a circuit board is required.

SUMMARY OF THE INVENTION

The object of the invention is to provide a circuit board wherein EMI noise emitted from the circuit board is reduced.

Another object of the invention is to provide a circuit board that can reduce noise mixed from an external device.

According to one aspect of the present invention, a substrate is provided which includes: pads which are provided on the surface of said substrate; and surface layers which are kept to the ground potential and cover the surface of said substrate except said pads and their peripheral.

According to another aspect of the present invention, a substrate is provided which includes: a part of circuit which is provided on the surface of said substrate; and a surface layers which are kept to the ground potential and cover the surface of said substrate except said part of circuit and its peripheral.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the invention will be made more apparent by the following detailed description and the accompanying drawings, wherein:

Fig. 1 is a perspective drawing showing a part of a circuit board equivalent to a first embodiment of the invention;

Fig. 2 is a sectional view viewed along a line A-A of the circuit board according to the invention shown in Fig. 1;

Fig. 3 is a perspective drawing showing a part of a circuit board equivalent to a second embodiment of the invention;

Fig. 4 is a sectional view viewed along a line B-B of the circuit board according to the invention shown in Fig. 3;

Fig. 5 is a perspective drawing showing a part of a circuit board equivalent to a third embodiment of the invention; and

Fig. 6 is a sectional view viewed along a line C-C of the circuit board according to the invention shown in Fig. 5.

In the drawings, the same reference numerals represent the same structural elements.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A first embodiment of the present invention will be

described in detail below.

Referring to Fig. 1, a circuit board 10 includes ground layers 12, 14 and 16. The ground layer 12 is provided on the upper surface of the circuit board 10. The ground layer 14 is provided on the lower surface of the circuit board 10. The ground layers 12 and 14 form plural surface layers of the circuit board 10. The ground layer 16 is provided inside the circuit board 10. Specifically, the ground layer 16 is one of plural internal layers included in the circuit board 10. The ground layer 16 is put between the ground layers 12 and 14. The ground layers 12, 14 and 16 are electrically connected to a stable ground such as the body of chassis. For example, the ground layers 12, 14 and 16 are made of copper. The ground layers 12, 14 and 16 are formed so that they have the thickness of, for example, approximately 0.035 millimeter.

The circuit board 10 includes signal layers 18 and 22 and a power supply layer 20. The signal layer 18 is put between the ground layers 12 and 16. The signal layer 22 is put between the ground layers 14 and 16. The power supply layer 20 is put between the ground layers 14 and 16. Insulating material is filled between these layers. For example, glass epoxy resin is used For the insulating material.

Pads 24a, 24b and 24c are provided on the upper surface of the circuit board 10. The pads 24a, 24b and 24c are used to electrically connect electronic parts mounted on the surface of the circuit board 10. The ground layer 12 is removed in parts in which the pads 24a, 24b and 24c are

respectively provided. That is, the ground layer 12 is formed in the whole area except the pads 24a, 24b and 24c and their peripheral areas on the upper surface of the circuit board 10. It is desirable that an interval between each pad 24a, 24b, 24c and the ground layer 12 is as narrow as possible in a range where no short circuit is caused. The ground layer 14 is uniformly formed in the whole area of the lower surface of the circuit board 10.

In this embodiment, plural pads are provided on the upper surface of the circuit board 10, however, plural pads may be also provided on both the upper and lower surfaces of the circuit board 10. In this case, the ground layer 14 is formed in the whole area except the plural pads and their peripheral areas on the lower surface of the circuit board 10.

Pads are provided by making a hole in the ground layer formed on the surface of the circuit board to supply power and a signal to an electronic circuit mounted on the surface of the circuit board. The pads and the power supply layer or the signal layer are electrically connected via wiring.

Referring to Fig. 2, via holes 26, 28 and 30 are formed inside the circuit board 10. The pad 24a is connected to the power supply layer 20 via the via hole 26 and power is supplied to an electronic part mounted on the upper surface of the circuit board 10. The pads 24b and 24c are connected to the signal layers 18 and 22 via the via holes 28 and 30, respectively. The pads 24b and 24c receive and transmit various electric information from/to an electronic part mounted on the upper surface of the circuit board 10.

Conductive elements 32 and 36 are provided between the ground layers 12 and 16. Conductive elements 34 and 38 are provided between the ground layers 14 and 16. The conductive elements 32, 36, 34 and 38 are conductive and electrically connect the ground layers 12 and 14. Concretely, the conductive element 32 electrically connects the ground layers 12 and 16. The conductive element 34 electrically connects the ground layers 16 and 14. The conductive element 36 electrically connects the ground layers 12 and 16. The conductive element 38 electrically connects the ground layers 16 and 14. The conductive elements 32, 36, 34 and 38 may be made of the same material as that of a signal conductor.

An electronic part mounted on the circuit board is provided with a ground pin that defines ground potential. The ground pin can be connected to any of the ground layers 12, 14 and 16, however, it is desirable that it is electrically connected to the ground layer 12 for convenience of wiring.

In the circuit board 10 in this embodiment, power is supplied from the power supply layer 20 provided inside the circuit board 10 to an electronic part mounted on the surface of the board and ground potential is defined by connecting the ground pin of the electronic part to the ground layer 12. Also, a signal is received or transmitted from/to an electronic circuit via signal conductors 18 and 22. Therefore, in the circuit board 10 in this embodiment, a digital signal is conducted in the signal conductors 18 and 22 arranged in the circuit board 10 and the circuit board 10 is formed so that the ground layers 12, 14 and 16 cover the

signal conductors 18 and 22. Therefore, less EMI noise is emitted from the circuit board 10.

The circuit board according to the invention is not limited to that in the embodiment described above and may be freely varied in a range of the invention. For example, the number of ground layers, power supply layers and signal layers respectively provided between the ground layers 12 and 14 may be arbitrary. Also, respective wiring for supplying power, ground and a signal can be also provided in the same layer.

Also, in the embodiment described above, the surface layer of the circuit board 10 is kept to ground potential, covers an area except the pad and the periphery and is composed of two sides of the ground layers 12 and 14 or four sides of the ground layers 12 and 14 and both sides of the board 10, however, the surface layer may be also composed of six sides of the ground layers 12 and 14, both sides of the board 10 and the front and back of the board 10.

In this embodiment, the pads 24 are formed on the upper surface of the circuit board 10, however, a part of a circuit, for example, a pad, a pattern and a via hole, may be also formed on the upper surface of the circuit board 10 in stead of the pads. In this case, the pad and the via hole are connected via the pattern, and the pad and a signal conductor in an internal layer transmit a signal via the via hole and the pattern.

Next, a second embodiment of the present invention will be described in detail. The second embodiment is characterized in that a ground layer on the upper surface and

a ground layer on the lower surface are electrically connected via a via hole. The other configuration is similar to that in the first embodiment.

Referring to Figs. 3 and 4, a circuit board 10a includes plural via holes 21 and 23. The via hole 21 electrically connects ground layers 12, 16 and 14. Conductive material is filled inside the via hole 21. The via hole 23 electrically connects the ground layers 12, 16 and 14. Conductive material is filled inside the via hole 23.

In this embodiment, the number of via holes is not particularly limited. Only one via hole may be provided to each side of the circuit board 10a. Plural via holes may otherwise be also provided to each side.

Next, a third embodiment of the present invention will be described in detail. The third embodiment is characterized in that a ground layer on the upper surface and a ground layer on the lower surface are electrically connected via a conductive layer formed on the side. The other configuration is similar to that in the first embodiment.

Referring to Figs. 5 and 6, a circuit board 10b is provided with conductive layers 40 and 42. The conductive layer 40 is provided to one side of the circuit board 10b and the conductive layer 42 is provided to the other side. Each of the conductive layers 40 and 42 electrically connect the ground layers 12 and 14. The conductive layers 40 and 42 may be made of the same material as that of the ground layers 12 and 14.

As described above, according to the invention, as the

ground layers are formed on the top surface and the bottom surface of the circuit board, EMI noise can be reduced. Also, as the ground layers are formed on the top surface and the bottom surface of the circuit board, noise mixed from an external device, which deteriorates a signal conducted in the signal layer, can be reduced. Also, as wiring for transmitting a signal is not formed on the top surface and the bottom surface of the circuit board, there is also effect that a value of characteristic impedance is readily standardized.

While this invention has been described in conjunction with the preferred embodiments described above, it will now be possible for those skilled in the art to put this invention into practice in various other manners.

WHAT IS CLAIMED IS:

1. A substrate comprising:

pads which are provided on the surface of said substrate; and

surface layers which are kept to the ground potential and cover the surface of said substrate except said pads and their peripheral.

2. The substrate as claimed in claim 1, wherein said surface layers includes a top main surface and a bottom main surface.

3. The substrate as claimed in claim 2, further comprising:

a conductive element which electronically connects said top main surface and said bottom main surface.

4. The substrate as claimed in claim 2, further comprising:

vias which electronically connects said top main surface and said bottom main surface.

5. The substrate as claimed in claim 4, wherein said vias are provided on the side portion of said substrate.

6. The substrate as claimed in claim 2, wherein said surface layers further includes a side layer which electronically connects said top main surface and said bottom main surface.

7. The substrate as claimed in claim 1, wherein said surface

layers includes six surface layers.

8. The substrate as claimed in claim 1, further comprising a signal layer which is provided between said top main surface and said bottom main surface, and has a pattern which is connected to at least one of said pads.

9. The substrate as claimed in claim 1, wherein an interval between said pad and said surface layer is defined to prevent said pad form short-circuiting.

10. A substrate comprising:

a part of circuit which is provided on the surface of said substrate; and

a surface layers which are kept to the ground potential and cover the surface of said substrate except said part of circuit and its peripheral.

11. The substrate as claimed in claim 1, wherein said surface layers includes a top main surface and a bottom main surface.

12. The substrate as claimed in claim 2, further comprising:

a conductive element which electronically connects said top main surface and said bottom main surface.

13. The substrate as claimed in claim 2, further comprising:

vias which electronically connects said top main surface and said bottom main surface.

14. The substrate as claimed in claim 4, wherein said vias are provided on the side portion of said substrate.

15. The substrate as claimed in claim 2, wherein said surface layers further includes a side layer which electronically connects said top main surface and said bottom main surface.

16. The substrate as claimed in claim 1, wherein said surface layers includes six surface layers.

17. The substrate as claimed in claim 1, further comprising a signal layer which is provided between said top main surface and said bottom main surface, and has a pattern which is connected to said part of circuit.

18. The substrate as claimed in claim 1, wherein an interval between said part of circuit and said surface layer is defined to prevent said part of circuit form short-circuiting.

Abstract

A substrate of the present invention includes pads which are provided on the surface of said substrate; and surface layers which are kept to the ground potential and cover the surface of said substrate except said pads and their peripheral. Another substrate of the present invention includes a part of circuit which is provided on the surface of said substrate; and a surface layers which are kept to the ground potential and cover the surface of said substrate except said part of circuit and its peripheral.

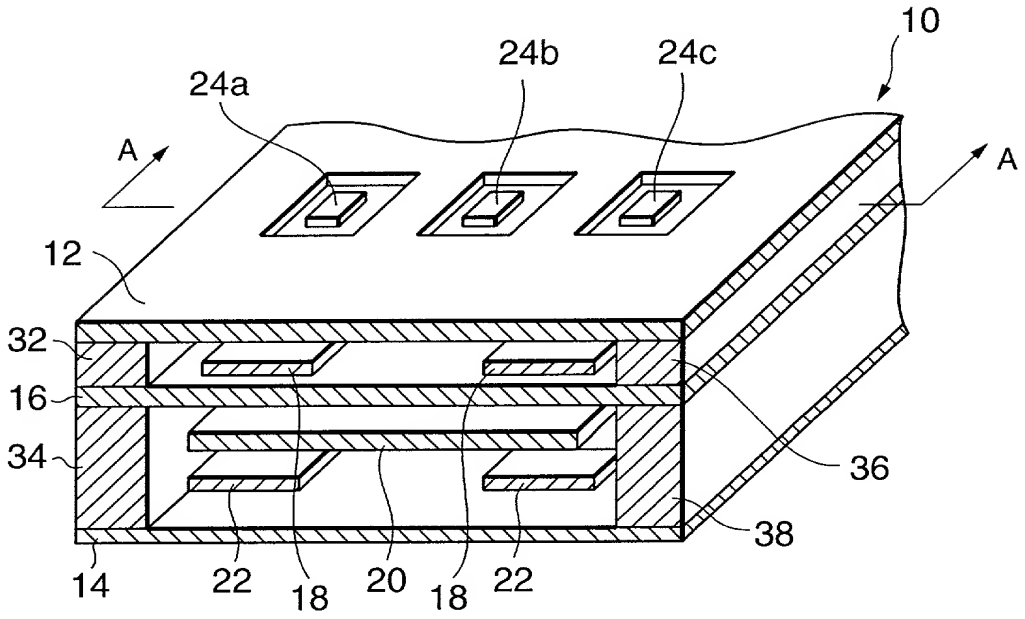
10
24a
24b
24c
A
A
12
32
16
34
36
38
14
22
18
20
18
22

Fig.1

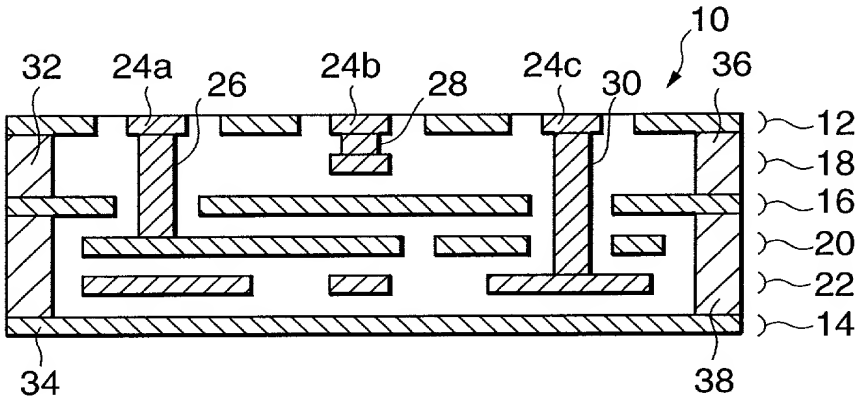
10
32
24a
26
24b
28
24c
30
36
12
18
16
20
22
14
34
38

Fig.2

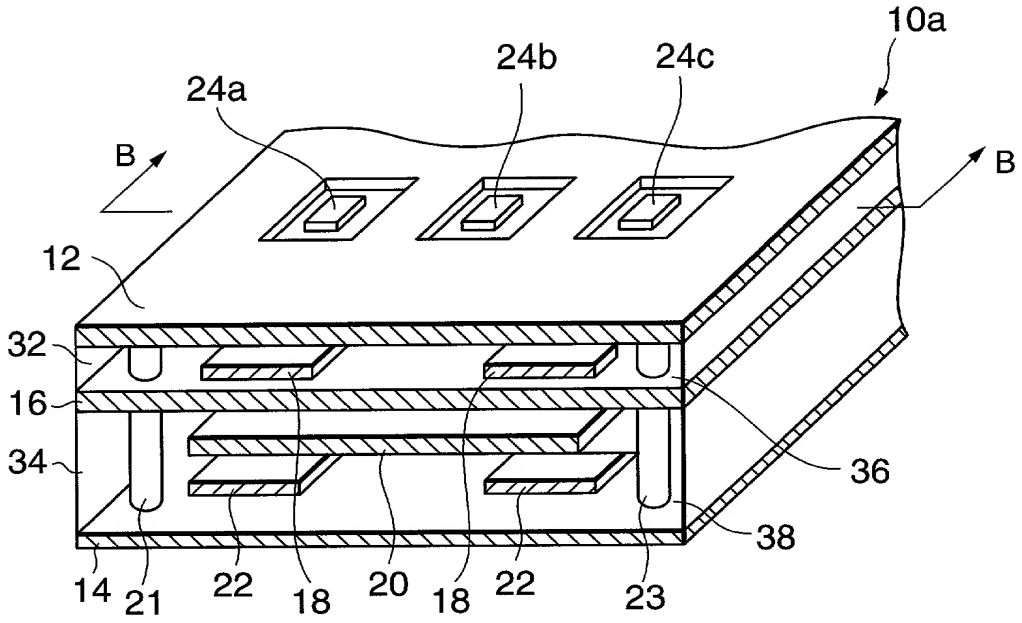
10a
24b
24c
24a
B
B
12
32
16
34
36
38
14
21
22
18
20
18
22
23

Fig.3

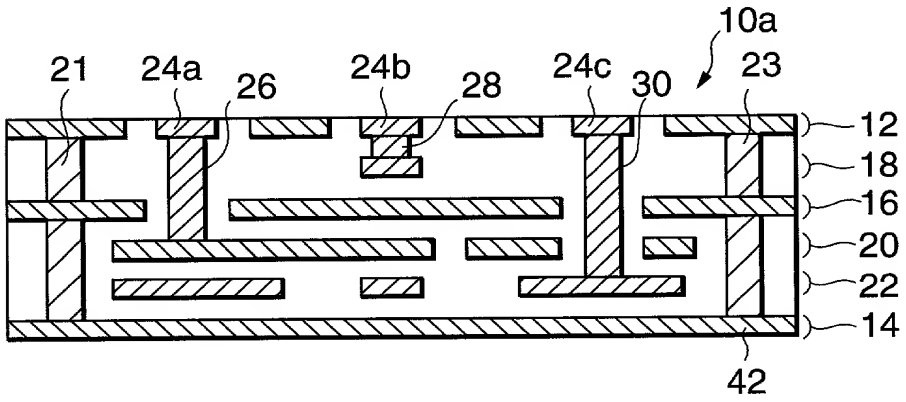
10a
21
24a
26
24b
28
24c
30
23
12
18
16
20
22
14
42

Fig.4

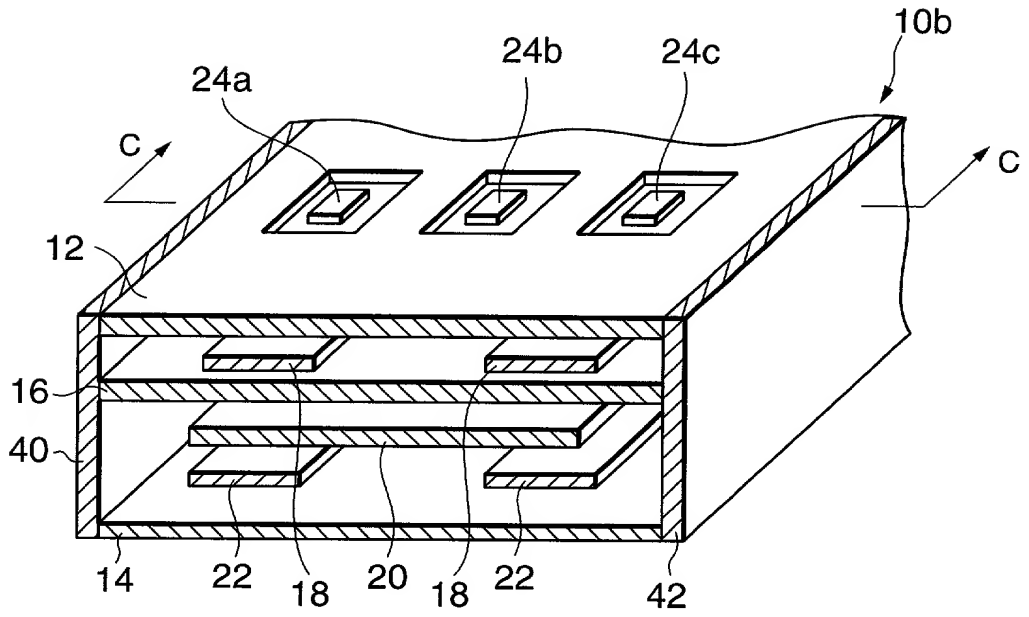
10b
24a
24b
24c
C
C
12
16
40
14
22
18
20
18
22
42

Fig.5

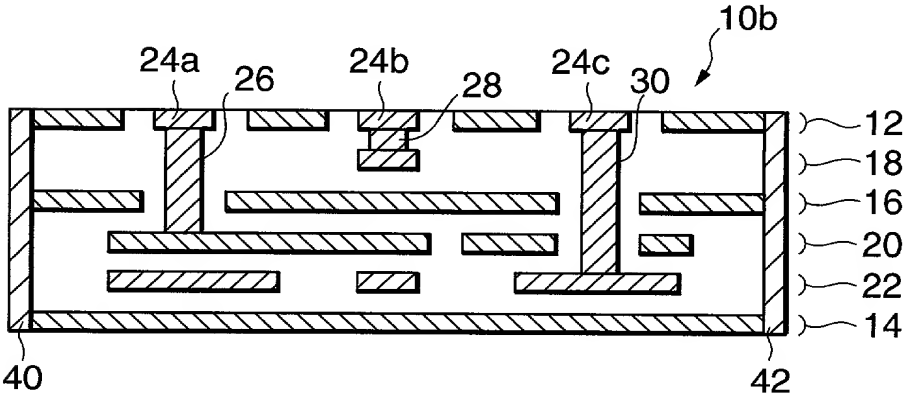
10b
24a
26
24b
28
24c
30
12
18
16
20
22
14
40
42

Fig.6

Declaration and Power of Attorney for Patent Application

特許出願宣言書

Japanese Language Declaration

私は、下欄に氏名を記載した発明として、以下の通り宣言する：

As a below named inventor, I hereby declare that:

私の住所、郵便の宛先および国籍は、下欄に氏名に続いて記載したとおりであり、

My residence, post office address and citizenship are as stated below next to my name,

名称の発明に関し、請求の範囲に記載した特許を求める主題の本来の、最初にして唯一の発明者である（一人の氏名のみが下欄に記載されている場合）か、もしくは本来の、最初にして共同の発明者である（複数の氏名が下欄に記載されている場合）と信じ、

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

_____

_____

_____

CIRCUIT BOARD

_____

_____

その明細書を
（該当するほうに印を付す）

the specification of which
(check one)

☐ ここに添付する。

☒ is attached hereto.

☐ _____ 日に出願番号

第 _____ 号として提出し、

☐ was filed on _____ as

Application Serial No. _____

_____ 日に補正した。
（該当する場合）

and was amended on _____
(if applicable)

私は、前記のとおり補正した請求の範囲を含む前記明細書の内容を検討し、理解したことを陳述する。

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37部第1章第56条(a)項に従い、本願の審査に所要の情報を開示すべき義務を有することを認める。

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Japanese Language Declaration

私は、合衆国法典第35部第119条、第172条、又は第365条に基づく下記の外国特許出願又は発明者証出願の外国優先権利益を主張し、さらに優先権の主張に係わる基礎出願の出願日前の出願日を有する外国特許出願又は発明者証出願を以下に明記する：

I hereby claim foreign priority benefits under Title 35, United States Code §119, §172 or §365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior foreign applications
先の外国出願

(Number) (番　号)	(Country) (国　名)	(Day/Month/Year Filed) (出願の年月日)	Priority claimed 優先権の主張 Yes あり	No なし
343955/1999	Japan	2/12/1999	☒	☐
			☐	☐
			☐	☐
			☐	☐
			☐	☐

私は、合衆国法典第35部第120条に基づく下記の合衆国特許出願の利益を主張し、本願の請求の範囲各項に記載の主題が合衆国法典第35部第112条第1項に規定の態様で先の合衆国出願に開示されていない限度において、先の出願の出願日と本願の国内出願日又はＰＣＴ国際出願日の間に公表された連邦規則法典第37部第1章第56条(a)項に記載の所要の情報を開示すべき義務を有することを認める。

I hereby claim the benefit of Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose any material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) (出願番号)	(Filing Date) (出願日)	(現　況) (特許済み、係属中、放棄済み) (Status) (patended, pending abandoned)

私は、ここに自己の知識に基づいて行った陳述がすべて真実であり、自己の有する情報及び信ずるところに従って行った陳述が真実であると信じ、更に故意に虚偽の陳述等を行った場合、合衆国法典第18部第1001条により、罰金もしくは禁固に処せられるか、又はこれらの刑が併科され、又はかかる故意による虚偽の陳述が本願ないし本願に対して付与される特許の有効性を損なうことがあることを認識して、以上の陳述を行ったことを宣言する。

I hereby declare that all statements made herein of my own knowledge are true; and further that all statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Japanese Language Declaration

委任状： 私は、下記発明者として、以下の代理人をここに選任し、本願の手続きを遂行すること並びにこれに関する一切の行為を特許商標局に対して行うことを委任する。
（代理人氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

I hereby appoint John H. Mion, Reg. No. 18,879; Donald E. Zinn, Reg. No. 19,046; Thomas J. Macpeak, Reg. No. 19,292; Robert J. Seas, Jr., Reg. No. 21,092; Darryl Mexic, Reg. No. 23,063; Robert V. Sloan, Reg. No. 22,775; Peter D. Olexy, Reg. No. 24,513; J. Frank Osha, Reg. No. 24,625; Waddell A. Biggart, Reg. No. 24,861; Robert G. McMorrow, Reg. No. 19,093; Louis Gubinsky, Reg. No. 24,835; Neil B. Siegel, Reg. No. 25,200; David J. Cushing, Reg. No. 28,703; John R. Inge, Reg. No. 26,916; Joseph J. Ruch, Jr., Reg. No. 26,577; Sheldon I. Landsman, Reg. No. 25,430; Richard C. Turner, Reg. No. 29,710; Howard L. Bernstein, Reg. No. 25,665; Alan J. Kasper, Reg. No. 25,426; Kenneth J. Burchfiel, Reg. No. 31,333; Gordon Kit, Reg. No. 30,764; Susan J. Mack, Reg. No. 30,951; Frank L. Bernstein, Reg. No. 31,484; Mark Boland, Reg. No. 32,197; William H. Mandir, Reg. No. 32,156; Scott M. Daniels, Reg. No. 32,562; Brian W. Hannon, Reg. No. 32,778; Abraham J. Rosner, Reg. No. 33,276; Bruce E. Kramer, Reg. No. 33,725; Paul F. Neils, Reg. No. 33,102; and Brett S. Sylvester, Reg. No. 32,765, my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and request that all correspondence about the application be addressed to SUGHRUE, MION, ZINN, MACPEAK & SEAS, PLLC, 2100 Pennsylvania Avenue, N.W., Washington, D.C. 20037-3202.

書類の送付先： Send Correspondence to:

SUGHRUE, MION, ZINN, MACPEAK & SEAS
2100 Pennsylvania Avenue, N.W., Washington, D.C. 20037

直通電話連絡先： （名称及び電話番号） Direct Telephone Calls to: *(name and telephone number)*

(202)293-7060

唯一の又は第一の発明者の氏名	Full name of sole or first inventor TAKASHI ABE
同発明者の署名 日付	Inventor's signature Date Takashi Abe 9/20/2000
住所	Residence Tokyo, Japan
国籍	Citizenship Japanese
郵便の宛先	Post office address c/o NEC Corporation, 7-1, Shiba 5-chome
	Minato-ku, Tokyo, Japan
第二の共同発明者の氏名（該当する場合）	Full name of second joint inventor, if any
同第二発明者の署名 日付	Second inventor's signature Date
住所	Residence
国籍	Citizenship
郵便の宛先	Post office address

（第三又はそれ以降の共同発明者に対しても同様な情報および署名を提供すること。）

(Supply similar information and signature for third and subsequent joint inventors.)